CLAIMS

1. A hardware unit (2) for operating memory components, which hardware unit (2) comprises a memory controller, a plurality of interface pins (3-6) and a bus connected to said memory controller and to said interface pins (3-6), said memory controller determines the number of memory components (21,31,41,42,51,52,61,62) external to said hardware unit (2) and connected to said interface pins (3-6), wherein in case at least one memory component (21,31,41,42,51,52,61,62) is determined to be connected to said interface pins (3-6), said memory controller divides the capacity of said bus into as many portions as there are connected memory components (21,31,41,42,51,52,61,62), allocates each portion to another group of said interface pins (3-6) to which a separate memory component (21,31,41,42,51,52,61,62) is connected, and exchanges signals via said bus and said interface pins (3-6) separately with each connected memory component (21,31,41,42,51, 52,61,62).

2. A hardware unit (2) according to claim 1, wherein said memory controller determines the number of memory components (21,31,41,42,51,52,61,62) external to said hardware unit (2) and connected to said interface pins (3-6) by retrieving a corresponding pre-determined value from storage means.

3. A hardware unit (2) according to claim 1, wherein said memory controller determines the number of memory components (21,31,41,42,51,52,61,62) external to said hardware unit (2) and connected to said interface pins

(3-6) in an identification cycle via said bus of said hardware unit.

4. A hardware unit (2) according to claim 1, wherein said memory controller supports an exchange of signals with at least one memory component (31,51,52,62) internal to an electronic device (1) comprising said hardware unit (2) and with at least one memory component (21,41,42,61) external to said electronic device (1).

5. A hardware unit (2) according to claim 1, wherein said memory controller supports an exchange of signals with memory components (21,31,41,42,51,52,61,62) with different speeds.

6. A hardware unit (2) according to claim 1, wherein said memory controller supports an exchange of signals with a single connected memory component (21,31) using the entire capacity of said bus.

7. A hardware unit (2) according to claim 1, wherein said memory controller applies the same interface protocol for any memory component connected to said interface pins (3-6).

8. A hardware unit (2) according to claim 1, wherein said memory controller multiplies control signals required for an exchange of data signals with memory components by the number of memory components determined to be connected to said interface pins (3-6).

9. A hardware unit (2) according to claim 1, wherein said interface pins comprise two groups of pins (3,4) for a

data exchange and two groups of pins (5,6) for an exchange of control signals with memory components (21,31,41,42,51,52,61,62).

10. A hardware unit according to claim 1, wherein said memory controller supports an identification cycle via said bus and said interface pins, in which identification cycle sub-components of a memory component connected to said interface pins are identified.

11. A hardware unit (2) according to claim 1, further comprising a unit for exchanging signals via said bus and said interface pins (3-6) with a device other than a memory component, which device is connected to said interface pins (3-6), in case no memory component is connected to said interface pins (3-6).

12. A hardware unit (2) according to claim 1, wherein said hardware unit (2) is a chip.

13. An electronic device (1) comprising a hardware unit (2) according to claim 1.

14. An electronic device (1) according to claim 13, further comprising at least one internal memory component (31,51,52,62) connected to said interface pins (3-6).

15. An electronic device (1) according to claim 13, further comprising at least one external interface (23,43,44,63) connected to said interface pins (3-6) for connecting an external memory component (21,41,42,61).

16. An electronic device (1) according to claim 13, wherein said electronic device (1) is a portable device.

17. A method for operating memory components (21,31,41,42,51, 52,61,62) connected to interface pins (3-6) of a hardware unit (2), which hardware unit (2) further comprises a memory controller and a bus connected to said memory controller and to said interface pins (3-6), said method comprising:
- determining the number of memory components (21,31,41,42,51, 52,61,62) connected to said interface pins (3-6);
- in case at least one memory component (21,31,41,42,51,52,61,62) is determined to be connected to said interface pins (3-6), dividing the capacity of said bus into as many portions as there are connected memory components (21,31,41,42,51,52,61,62) and allocating each portion to another group of said interface pins (3-6) to which a separate memory component (21,31,41,42,51,52,61,62) is connected; and
- exchanging signals between said memory controller and each memory component (21,31,41,42,51, 52,61,62) connected to said interface pins (3-6) separately via said bus and said interface pins (3-6).

18. A method according to claim 17, wherein said step of determining the number of memory components (21,31,41,42,51, 52,61,62) connected to said interface pins (3-6) comprises retrieving a corresponding pre-determined value from storage means.

19. A method according to claim 17, wherein said step of determining the number of memory components (21,31,41,42,51, 52,61,62) connected to said interface pins (3-6) comprises performing an identification cycle via said bus of said hardware unit (2).

20. A method according to claim 17, wherein the same interface protocol is applied for any memory component (21,31,41,42,51,52,61,62) connected to said interface pins (3-6).

21. A method according to claim 17, comprising multiplying control signals required for an exchange of data signals with memory components by the number of memory components determined to be connected to said interface pins.

22. A method according to claim 17, further comprising performing an identification cycle via said bus and said interface pins, in which identification cycle sub-components of each memory component connected to said interface pins are identified.